Characterization and Application of Nanomaterials 2024, 7(2), 6236.
https://doi.org/10.24294/can.v7i2.6236

Article

Reversible logic-based parity generator circuit for nano communication network using QCA

Sravan K. Vittapu*, Ravichand Sankuru, Ravi Bolimera, Kuruva Madhu Ramudu, Mekala Rameshwar Reddy, Maddula Manasa Reddy

Department of Electronics and Communication Engineering, Nalla Narasimha Reddy Education Society's Group of Institutions, Hyderabad 500088, Telangana, India
*** Corresponding author:** Sravan K. Vittapu, vsravan91@gmail.com

CITATION

Vittapu SK, Sankuru R, Bolimera R, et al. Reversible logic-based parity generator circuit for nano communication network using QCA. Characterization and Application of Nanomaterials. 2024; 7(2): 6236. https://doi.org/10.24294/can.v7i2.6236

ARTICLE INFO

Received: 6 May 2024
Accepted: 8 July 2024
Available online: 26 July 2024

Abstract: An alternative to CMOS VLSI called Quantum Cellular Automata (QCA) is presently being researched. Although a few basic logical circuits and devices have been examined, very little, if any, research has been done on the architecture of QCA device systems. In the context of nano communication networks, data transmission that is both dependable and efficient is still critical. The technology known as Quantum Dot Cellular Automata (QCA) has shown great promise in the development of nano-scale circuits because of its extremely low power consumption and rapid functioning. This study introduces a unique nano-communication parity-based arithmetic circuit that is reversible, error-detecting, and error-correcting. The minimal outputs are needed for the proposed structure. Based on QCA technology, the proposed nano-communication network makes use of reversible logic gates. The performance increase of the suggested parity generator and checker circuit is significant in terms of clock delay, size, and number of cells.

Keywords: CMOS; nano communications networks; parity generator; parity checker; reversible logic; VLSI

1. Introduction

Given that people must utilise electronics, it is regrettable that common electronic gadgets based on CMOS technology have flaws. There are some significant drawbacks to this technique, such as short-channel effects. As CMOS technology nears its physical limits, issues like power dissipation and the quantum effect are becoming more noticeable. The design complexity increases much further when CMOS technology is down to the nanoscale. Reversibility processing is one of the most important subjects in nanotechnology, the science that complements CMOS technology. This is due to the physical constraints of CMOS technology, which include its larger dimensions compared to QCA. We work on both hardware and software components to attain great efficiency. Power analysis is therefore important since it can assist designers in identifying the positive long-term consequences [1].

On the whole, circuit designers were able to construct new goods utilising QCA technology because the logic value model relies on where electrons are located in each cell of quantum dots. The zero-and-one logic paradigm in CMOS is based on low and high voltages. Irreversible logic generally causes some input data to be lost, which could lead to increased power consumption. When this happens, the output information is not recoverable, so we must retrieve the data from the main memory [2,3]. According to Landauer's research, every bit of information lost results in the

loss of KTLn2 joules of heat energy, where T is the operation's absolute temperature and K is Boltzmann's constant [4]. A circuit must be made up of reversible gates in order to prevent this energy dissipation [5]. Energy dissipation is decreased by reversible logic, which produces a one-to-one connection between input and output vectors. Reversible computing is limited primarily by minimising the quantum cost, minimising input constants, minimising garbage outputs, and employing the fewest number of gates possible [6,7]. Parity and Feynman diagrams are crucial components of arithmetic computing [8]. This study proposes an optimised reversible Feynman design implementation using parity generators, parity checker gates, and the efficient XOR proposed by Ahmed and Naz [8]. To show expandability, we then create a nano communication design with fewer garbage outputs. Moreover, the proposed nano-communication designs are reversible and provide fault tolerance.

2. Related works

The design of the Nano Communication Network Reversible Based Parity Generator Circuit Using QCA has involved numerous research projects. Below is a discussion of some of them. Numerous issues and inadequacies have been noted in recent decades as a result of the emergence of significant limitations on the complementary metal oxide semiconductor (CMOS) technology's capacity to scale physically. A few of the challenges that come with this technology are short channel effects and high leakage power consumption. Reversible gates are used in conjunction with a procedural technique in the study of Bagherian Khosroshahy et al. [1] to minimise latency in the system design, which is based on output conformance and a requirements self-checking approach. The reversibility logic will be the focus of the suggested circuit. In comparison to the study of Danehdaran et al. [2], the technique is obtained with enhanced reliability. Since there is no fan-out in the reversible logic gates, there is no power dissipation [3]. The output terms and garbage values are both present in the reversible logic. The relationship between the trash value, the input, and the output [4]. The primary parameters to be discussed in reversible logic are quantum cost, garbage, constant input, and latency. Every circuit needs a delay calculation feature in order to adjust efficiency. The parity generator circuit implements a novel Feynman-based, reversible, and fault-tolerant nano communication arithmetic architecture with several trash outputs [5].

According to Panahi et al.'s research, every bit of information lost results in the loss of KTLn2 joules of heat energy, where T is the operation's absolute temperature and K is Boltzmann's constant [6]. Reversibility is crucial for error detection in nano-circuits since it allows for lossless transmission and the absence of data loss. Additionally, latency and cell count are not described independently in the majority of these irreversible circuits. Although their circuits contain more cells and a delay, the parity generator, parity checker, and their nano-communication circuit have been created reversibly using odd parity bits in the study of Panahi et al. [7]. Feynman and parity are crucial components of arithmetic computing in the study of Ahmed and Naz [8]. The suggested Feynman gate uses an XOR gate based on Ahmed and Naz [8], despite certain limitations in cell placement leading to greater overhead areas. Equation [9] can be used to calculate the electrostatic interaction force between each

cell's two electrons. QCA technology flaws are mostly associated with the deposition process, which may be classified into four distinct kinds [10–14]. The transmitted data from the parity generator is controlled by the odd parity checker, which verifies its accuracy. An error during transmission will occur if the parity output of the four bits (the three message bits plus the parity bit) is even. As a result, the binary information that was originally transferred was strange [12,15–17]. In the study of Mohaimeed and Rabee [18], new nano composite thin films were fabricated that outperformed TiO_2 films in terms of transmittance and energy gap. In the study of Najm et al. [19], a new technique was employed named solvothermal, which is used for the deposition of nano particles into nano thin films.

Figure 1 shows a high-level representation of a four-dot QCA cell. A square is created by positioning four quantum dots. Little semi-conductor or metal islands known as quantum dots have a diameter that is small enough to cause their fluctuating energy to be more than KBT (where T is the operating temperature and KB is Boltzman's constant). (They will eventually shrink to fit within specifically made molecules.) They will trap individual charge barriers if this is the case.

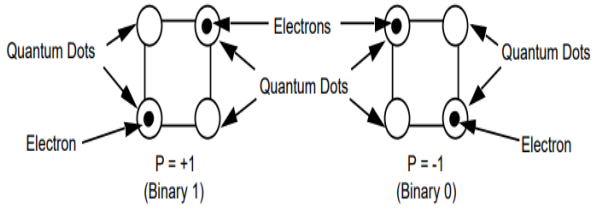

Figure 1. QCA cell polarization and representations of binary 1 and binary 0.

Through electron tunnelling, exactly two mobile electrons are loaded into the cell and are able to travel to various quantum dots within the QCA cell. In 2.1, the lines that join the quantum dots depict the tutoring routes. The electrons will only occupy the corners of the QCA cell due to repulsion, creating two distinct polarisations. There are two types of cells with 90° and 45° rotations that are commonly used in semiconductor QCA technology. Both types can be represented as zero and one logic, but there is a slight variation in the forms of the cells that are placed, even though each cell's computation remains the same. A 90° cell would become a 45° cell if it were rotated by 45°. It is assumed that potential barriers between neighbouring QCA cells, which are raised and lowered by capacitive plates, provide total control over electron tunnelling.

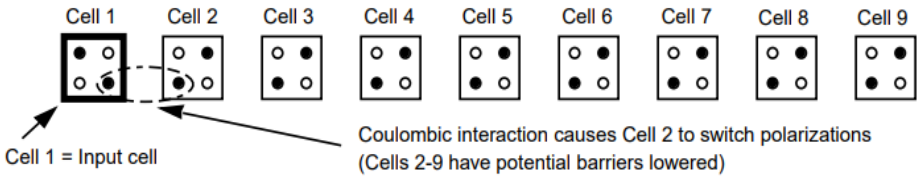

Figure 2. A QCA wire.

A QCA wire depicted in **Figure 2** is created by electrostatic interaction between cells arranged in a row next to one another; any input value can propagate across the wire, and the output cell will have a value equal to the input cell. Because of this, each

cell can perform the three important functions of wire, processor, and memory all at once.

Generally speaking, a lot of work has gone into creating an inverter gate, as shown in **Figure 3**. All the gates are identical in terms of functioning, but because they are utilised for distinct purposes, each inverter gate has a unique map and overall design. Random input values are applied to the input cell of every inverter gate. Based on the electrostatic interactions between electrons, any amount of propagation on a gate occurs in between. This is caused by a change in the middle cell's placement, which charges the middle values in the opposite direction. The output cell then provides the reverted value.

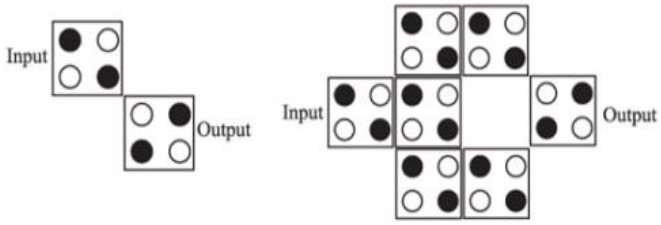

Figure 3. Inverter gate.

Potential barriers (that would be beneath the cell) that can be increased and reduced between neighbouring QCA cells using capacitive plates are considered to be the only means of controlling electron tunnelling.

Majority gate:

The majority and inverter gates are essential gates in QCA technology that designers can utilise to create any kind of new circuit. There should be an odd number of cells in the majority. We now want to talk about a three-input majority gate, which has three inputs, one voter cell, and one output cell—as the name suggests. The function of this gate is indicated in Equation. The majority gate and the inverter gate share the same electrostatic interactions. The structure of the three input majority gates is shown in **Figure 4**.

$$\text{Majority} = AB + BC + AC \quad (1)$$

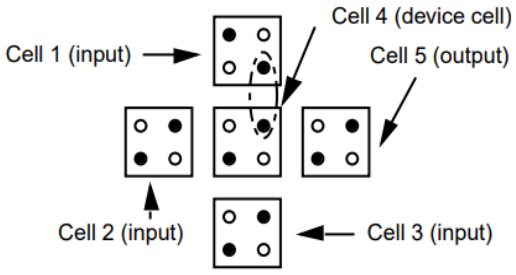

Figure 4. The fundamental QCA logical device—The majority gate.

3. The proposed method

3.1. The reversible Feynman gate

More energy is being used by computers than ever before, with over a billion of them in use globally. Computers with reversible features can use less power in several areas, such as the CPU and memory. To run on a computer, a process has to divide the

calculation into smaller units. Reversible hardware ensures that no result is wasted since occasionally, for a process or set of pieces to be completed, it requires the other parts. Therefore, fetching from main memory is not necessary. When a CPU based on reversible hardware executes instructions, for instance, middle registers do not need to keep the results of prior computations; this helps to lower a device's energy consumption and overall calculation time.

Reversible circuit design has generally received far more attention in recent decades [13]; the Feynman gate is one of the most well-known reversible arithmetic logic gates. One of the numerous circuits that can use the Feynman gate is the ALU. The Feynman gate is a two-by-two device with two inputs, *A* and *B*, and two outputs, *Q* and *P*. The correspondence between the inputs and outputs is one to one. $P = A$ and $Q = (A \oplus B)$ are the respective output equations. When $A = 0$ and B = 0, this gate's functioning would result in $P = 0$ and $Q = 0$ as output. In a similar vein, if $A = 0$ and $B = 1$, the result would be $P = 0$ and $Q = 1$, and the cycle would repeat. The reversible Feynman gate suggested by the QCA layout is depicted in **Figure 5**.

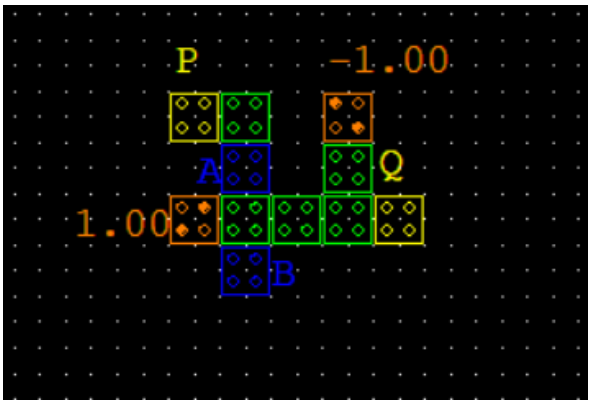

Figure 5. Layout of Feynman gate.

3.2. The reversible odd-parity generator and checker

When designing circuits, the most crucial element is extensibility. A reversible parity generator and checker circuit's complexity is dependent on several variables and necessitates careful evaluation of performance trade-offs. Among the methods most frequently employed for data transmission fault detection is the parity-generating technique. Binary data in digital systems is susceptible to noise during transmission and processing, which can change 0 s (of the data bits) to 1 s and 1 s to 0 s. Below is a block schematic of the parity generator depicted in **Figure 6**.

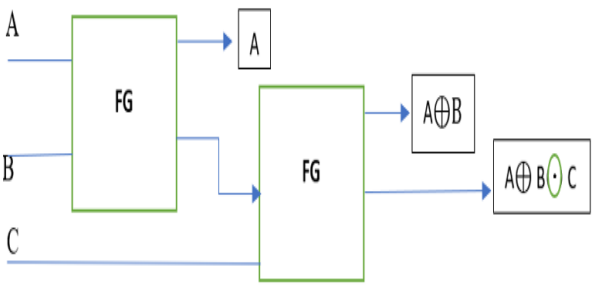

Figure 6. Block diagram of odd-parity generator.

Therefore, to make the number of 1 s even or odd, a parity bit is added to the word containing the data. A new reversible odd-parity generator is shown to illustrate the benefit. It has three inputs, *X*1, *X*2, and *X*3, and one output parity bit. The odd-parity generator's QCA configuration is displayed in **Figure 7**. One way to characterise the suggested 3-bit reversible gate is as follows:

$$X1 = \text{GAR } 1 \quad (2)$$

$$X2 = \text{GAR } 2 \quad (3)$$

$$\text{X3(parity)} = X1 \text{ xor } (X2 \text{ xnor } X3) \quad (4)$$

The schematic of the parity checker is shown in **Figure 8**.

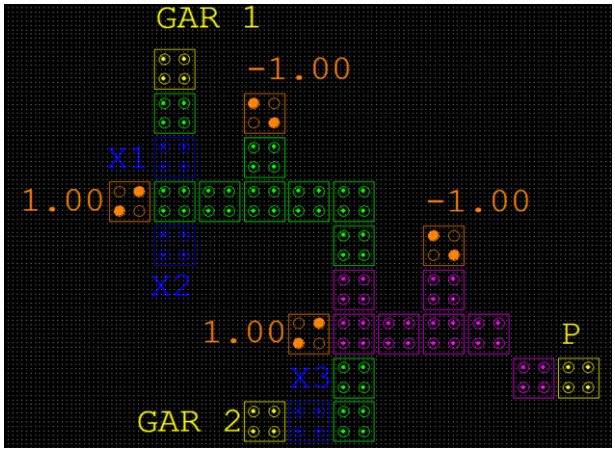

Figure 7. The schematic of the parity generator.

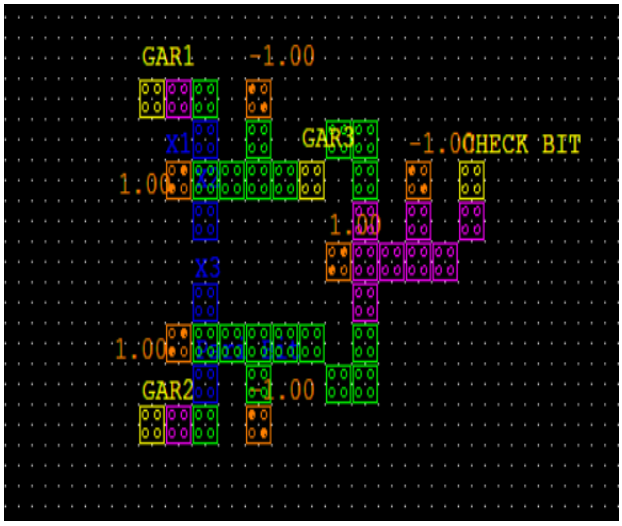

Figure 8. Layout of parity checker.

The odd-parity generator yields GAR1 = 0, GAR2 = 0, and a parity bit of 1 if *X*1 = 0, *X*2 = 0, and *X*3 = 0. On the other hand, the outputs become GAR1 = 0, GAR2 = 0, and parity bit = 0 when the inputs are *X*1 = 0, *X*2 = 0, and *X*3 = 1. The entire set of combinations for this generator is shown in **Table 1**. A circuit known as a parity checker is used to verify the receiver's parity. Check bit = 1 indicates an error occurs when the data word (three input bits plus the parity bit) turns even; check bit = 0 indicates no error occurs. The parity checker generates one output from four inputs

(*X*1, *X*2, *X*3, and the parity bit). The mathematics for this circuit, which the parity checker uses, are displayed below.

$$X1 = \text{GAR } 1 \quad (5)$$

$$X2 = \text{GAR } 2 \quad (6)$$

$$X3 = \text{GAR } 3 \quad (7)$$

$$\text{Check bit} = ((X1 \text{ xor } X2)' \text{ xor } (X3 \text{ xor parity bit})')' \quad (8)$$

Table 1. Truth table of the parity generator and parity checker system.

*X*1	*X*2	*X*3	Check bit	Parity bit	GAR1	GAR2
0	0	0	0	1	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	1	0	1
1	0	0	0	0	1	0
1	0	1	0	1	1	0
1	1	0	0	1	1	1
1	1	1	0	0	1	1

3.3. The proposed nano-communication system

Generally speaking, vulnerabilities in communications networks can be found by utilising a nano-communication system constructed with checkers and parity producing units. The three proposed components for nano-communication are the transmitter, the transmission medium, and the receiver. We solely used fault-tolerant components when designing the suggested nano-communication system, like fault-tolerant inverters and XOR [11].

- In addition to the three-input message, the transmitter generates a second bit known as the parity bit. The transmitted bit pattern has an odd number of 1s, or odd parity.
- The communication link between the source and the destination is provided by the transmission medium. The transmission medium (communication channel) is used to send the transmission bit pattern that the transmitter generates to the receiver.
- The receiver takes the transmission message word that the transmitter sent, along with the parity bit. At the receiver, the parity bit is examined in order to detect errors. An error has occurred through the transmission medium, indicating that one bit has changed if the received transmission bit pattern contains an even number of 1. If not, there has been no error.

Since actual clocking can lower fabrication costs and simplify the physical design, designing circuits based on it is a crucial component. Implementing QCA circuits based on real clocking has been the subject of numerous attempts; some solutions have been developed in a dynamic approach, while others have been built in a pipeline fashion [14]. Therefore, the pipeline format approach in the study of Jain et al. [14] would be the optimum option in the event of a loop-less circuit where the clock phase placement is sorted in increasing order. This has been taken into consideration in the case of the suggested nano-communication circuits, and the fundamental ideas

of our suggested technique readily apply to actual clocking. QCA schematic of the overall nano communication network is shown in **Figure 9**. In **Figures 10–12** show the simulation results of each block as depicted in **Figure 9**.

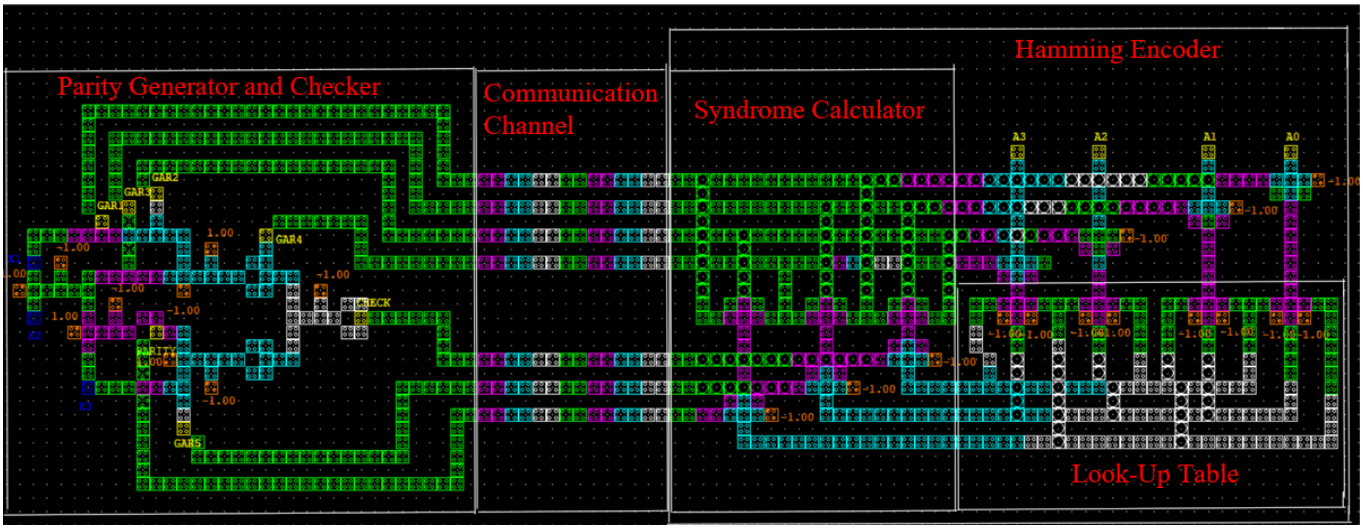

Figure 9. QCA circuit diagram of nano communication circuit.

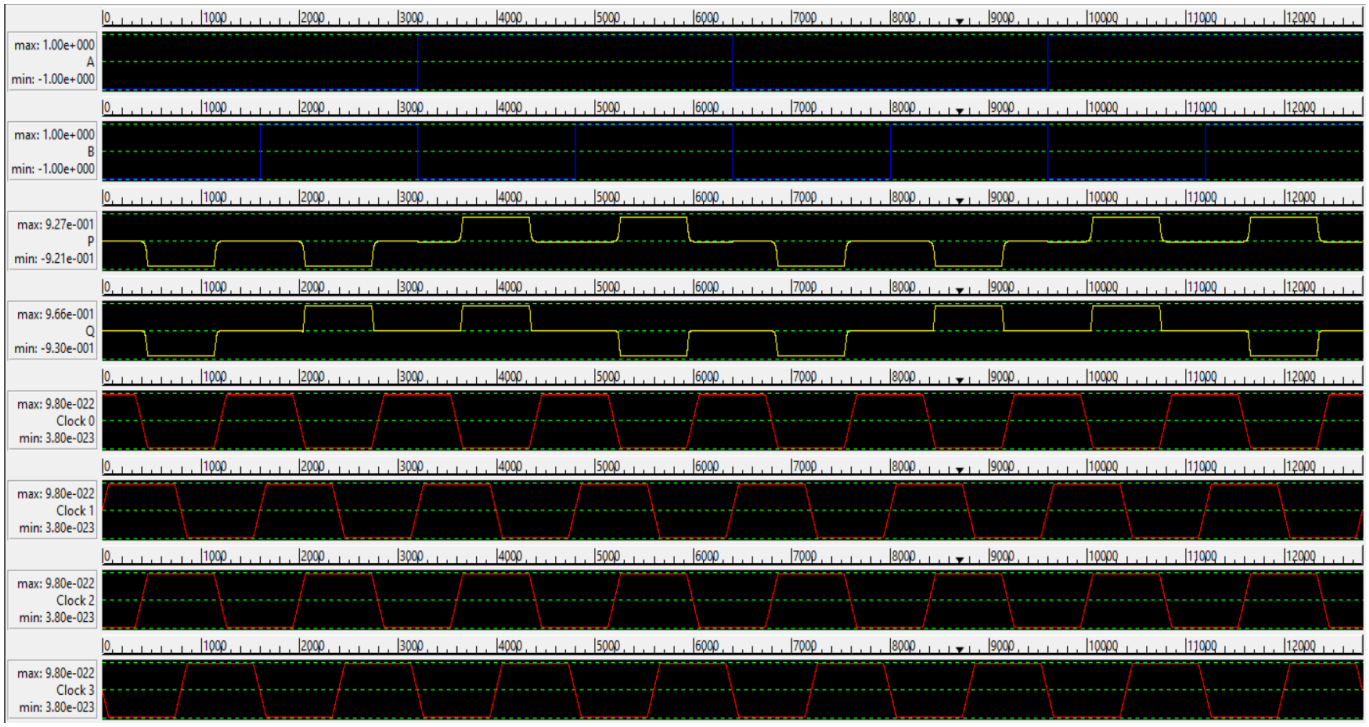

Figure 10. Simulation waveforms of Feynman gate.

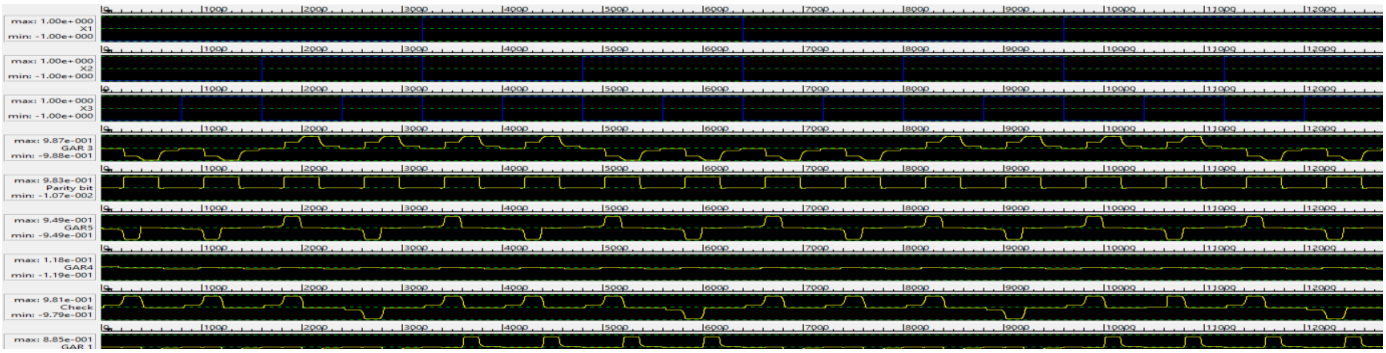

Figure 11. Simulation of parity generator and checker.

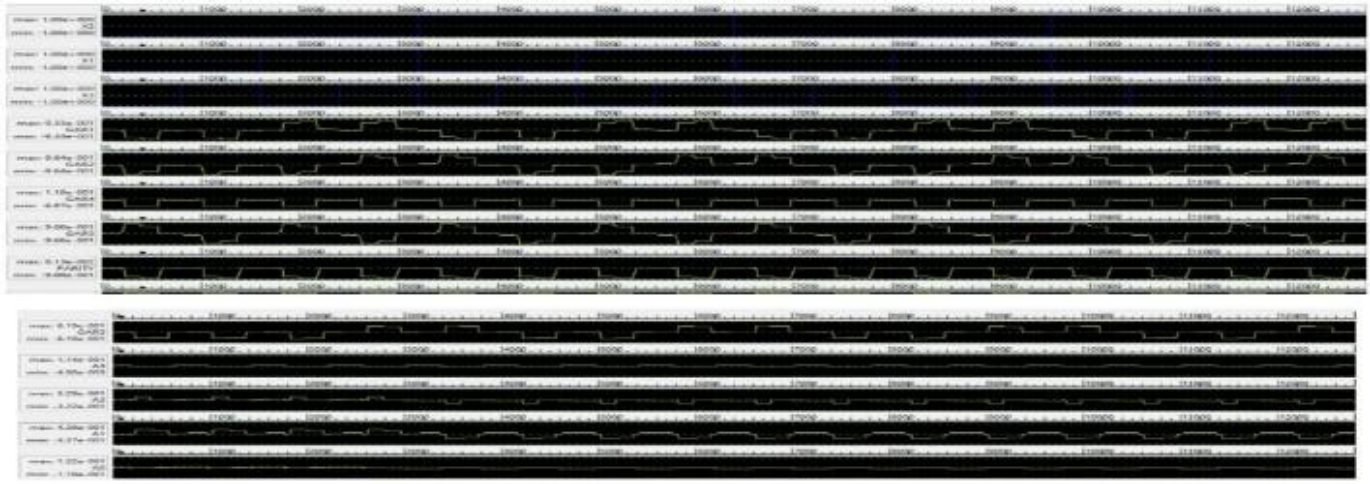

Figure 12. Simulation of nano communication circuit.

4. Experimental results

Performance evaluation and simulation results:

The most potent programme for simulating circuits based on QCA technology is QCA Designer. QCA cell size = 18 nm, quantum dot diameter = 5 nm, number of samples = 50,000, convergence tolerance = 0.001, radius of effect = 65 nm, relative permittivity = 12.9, clock low = 3.8×10^{-23} J, clock high = 9.8×10^{-22} J, clock amplitude factor = 2.000, layer separation = 11.5 nm, and maximum iterations per sample = 100 are some of the simulation parameters for this well-known tool.

5. Conclusion

In summary, a major advancement in the fields of nanotechnology and communication systems has been made with the design of the Nano Communication Network Reversible Based Parity Generator Circuit employing QCA. Through the utilisation of Quantum-dot Cellular Automata (QCA) special features, this circuit presents a viable path towards effective nanoscale data processing and transmission. In addition to guaranteeing low energy consumption (31.2%), its reversible design improves data transmission reliability by enabling error detection through parity creation. This method highlights the potential of nanotechnology to transform a number of industries, such as biomedical devices, the Internet of Things, and more, thereby influencing the direction of communication networks in the future. Building strong, high-performing systems in the nanoscale world requires the integration of

QCA-based circuits, such as the reversible parity generator, as we continue to explore the domain of nano communication.

Author contributions: Conceptualization, SKV and KMR; methodology, SKV, RS and RB; software, KMR, MRR and MMR; validation, SKV, RA and RB; formal analysis, KMR; investigation, SKV; resources, KMR; data curation, SKV and RS; writing—original draft preparation, SKV; writing—review and editing, SKV, RS and RB; visualization, KMR; supervision, SKV; project administration, KMR, MRR and MMR. All authors have read and agreed to the published version of the manuscript.

Conflict of interest: The authors declare no conflict of interest.

References

1. Bagherian Khosroshahy M, Abdoli A, Panahi MM. Novel Feynman-Based Reversible and Fault-Tolerant Nano-communication Arithmetic Architecture Based on QCA Technology. SN Computer Science. 2021; 2(6). doi: 10.1007/s42979-021-00811-5
2. Danehdaran F, Angizi S, Bagherian Khosroshahy M, et al. A combined three and five inputs majority gate-based high performance coplanar full adder in quantum-dot cellular automata. International Journal of Information Technology. 2019; 13(3): 1165-1177. doi: 10.1007/s41870-019-00365-z
3. Ahmad F, John MU, Khosroshahy MB, et al. Performance evaluation of an ultra-high speed adder based on quantum-dot cellular automata. International Journal of Information Technology. 2019; 11(3): 467-478. doi: 10.1007/s41870-019-00313-x
4. Landauer R. Irreversibility and heat generation in the computing process. IBM Journal of Research and Development. 2000; 44(1.2): 261-269. doi: 10.1147/rd.441.0261
5. Bennett CH. Logical Reversibility of Computation. IBM Journal of Research and Development. 1973; 17(6): 525-532. doi: 10.1147/rd.176.0525
6. Panahi MM, Hashemipour O, Navi K. A novel design of a ternary coded decimal adder/subtractor using reversible ternary gates. Integration. 2018; 62: 353-361. doi: 10.1016/j.vlsi.2018.04.014
7. Panahi MM, Hashemipour O, Navi K. A novel design of a multiplier using reversible ternary gates. IEEE.
8. Ahmed S, Naz SF. Notice of Violation of IEEE publication principles: design of cost efficient modular digital QCA circuits using optimized XOR Gate. IEEE Trans Circ Syst II Express Briefs. 2020.
9. Srivastava S, Sarkar S, Bhanja S. Estimation of Upper Bound of Power Dissipation in QCA Circuits. IEEE Transactions on Nanotechnology. 2009; 8(1): 116-127. doi: 10.1109/tnano.2008.2005408
10. Vankamamidi V, Ottavi M, Lombardi F. Two-Dimensional Schemes for Clocking/Timing of QCA Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2008; 27(1): 34-44. doi: 10.1109/tcad.2007.907020
11. Walus K, Dysart TJ, Jullien GA, et al. QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata. IEEE Transactions on Nanotechnology. 2004; 3(1): 26-31. doi: 10.1109/tnano.2003.820815
12. Das JC, De D. Quantum-dot cellular automata based reversible low power parity generator and parity checker design for nanocommunication. Frontiers of Information Technology & Electronic Engineering. 2016; 17(3): 224-236. doi: 10.1631/fitee.1500079
13. Thapliyal H, Ranganathan N. Reversible Logic-Based Concurrently Testable Latches for Molecular QCA. IEEE Transactions on Nanotechnology. 2010; 9(1): 62-69. doi: 10.1109/tnano.2009.2025038
14. Jain V, Sharnma DK, Gaur HM, et al. Comprehensive and comparative analysis of QCA-based circuit designs for next-generation computation. ACM Computing Surveys. 2023; 56(53): 1-36.
15. Sardinha LHB, Costa AMM, Neto OPV, et al. NanoRouter: A Quantum-dot Cellular Automata Design. IEEE Journal on Selected Areas in Communications. 2013; 31(12): 825-834. doi: 10.1109/jsac.2013.sup2.12130015
16. Yao F, Zein-Sabatto MS, Shao G, et al. Nanosensor Data Processor in Quantum-Dot Cellular Automata. Journal of Nanotechnology. 2014; 2014: 1-14. doi: 10.1155/2014/259869
17. Kamaraj A, Abinaya, Ramya S. Design of router using Reversible Logic in Quantum Cellular Automata. 2014 International Conference on Communication and Network Technologies. 2014. doi: 10.1109/cnt.2014.7062764

18. Mohaimeed AA, Rabee BH. Influence of Berry dye on some properties of nanocomposite (PVA/TiO2) films. Optical and Quantum Electronics. 2023; 55(3). doi: 10.1007/s11082-022-04523-9
19. Najm AAA, Alshrefi SM, Hadi ZL, et al. Synthesis of Novel [CdO(75%)/VO2(20%)/SiC(4%): p-Si] Heterojunction Composite Thin Films Decorated with Chlorophyll using Solvothermal-Laser Dual Technique for Solar Cell Applications. Silicon. 2024. doi: 10.1007/s12633-024-02997-8